

# ING916X Hardware Design Guide

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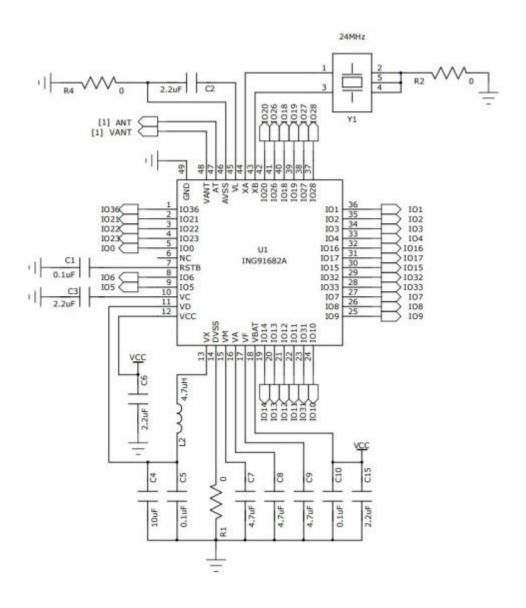
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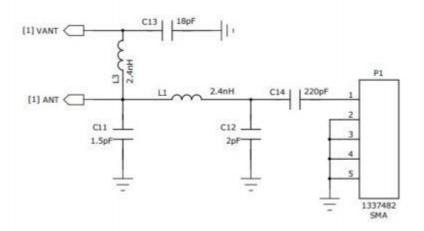
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# Reference circuit







### - Power Supply

The chip supports 1.62-3.63V DC power supply. The recommended power supply voltages from tech process are 1.8V, 2.5V and 3.0V. One 0.1u and one 2.2u capacitor are hung on the PCB near the VBAT pin. If conditions permit, the power input can increase the capacitance to suppress power.

### 二、DCDC periphery

- The ground DVSS of DCDC is connected to the chip ground through a 0 ohm resistance, and the DCDC uses a 4.7uH inductor..
- The routing of DCDC related pins shall be as short as possible and wide as possible.

## 三、Internal pull-up/down

The RSTB pin has a pull-up resistance (about 10k) inside the chip to the power supply.

#### 四、ADC

ADC reference voltage VREFP is connected to VBAT and VREFN is connected to GND. There is PGA module inside ADC. The voltage range that cannot be measured by PGA is VREFN~VREFP(0~VBAT), the corresponding sampling value is 0x0~0x3FFF; Enable PGA to measure the voltage range and magnification. Internal PGA magnification can be configured through register. The larger the magnification, the higher the resolution, but the smaller the measurement range. The voltage corresponding to the single ended mode sampling value 0x2000 is (VREFP + VREFN) / 2.

The voltage corresponding to differential mode sampling value 0x2000 is AIN\_P = AIN No.

A sampling channel in ADC is connected to the 1.2V regulated reference source, so that the reference voltage can be inversely calculated by sampling 1.2V( Voltage of VBAT) .

ADC Sampling Attentions to Suppress Power Supply Interference in Circuit Design, Measures that can be adopted include: adding filter capacitor to the power supply, short wiring and symmetrical shielding, using differential mode to suppress common mode noise, etc.

If the internal resistance of the signal source is relatively large, a drive shall be added between the signal and ADC.

# 五、Pin use as GPIO or peripheral



Peripherals are not fully mapped in GPIO, Which GPIOs can the corresponding peripherals be configured, Refer to the section Pin Controller in the chip data manual.

## 六、UART software upgrade

The following four signal lines are required for firmware upgrade through the serial port: EXTINT, RSTB, GPIO2 and GPIO3. PCB upper reserved ING916X chip hardware design guidance. The test points of these four signals are convenient for burning and debugging.

ullet If the master needs to be upgraded through the master MCU in the application, these signal

lines also need to be controlled by the MC.

•GPIO 0, GPIO 1 and GPIO 2 are no different from other GPIOs in normal operation, and can be used as common GPIOs and Peripheral interface.

## 七、4M Crystal

24M crystal determines the frequency offset of RF.

The load capacitance value (on chip load cap of the XO) inside the chip can be adjusted through the register. To change the crystal model, readjust the load capacitance value and test.

Pay attention to isolation in crystal pcb design (Wrapping crystals and related wires with gnd) .

Main parameters of 48M crystal:

Load Capacitance: 7.5pF-10pF.

For example:

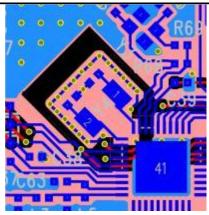
● Shenzhen Yangxing Technology Co., Ltd, 晶体型号: X201624MMB4SI, parameter: 24.000MHZ 10PF ±10PPM

# 八、32K Crystal

32k can use either the RC inside the chip or the external 32K crystal, Generally, 32k inside the chip can meet most applications. After software calibration, the 24-hour deviation is 2-3 seconds.

In other cases, if external 32K crystal pcb is used, pay attention to isolation to avoid infection (Wrap 32K related wiring with gnd).





## 九、Transmission Power

The chip can set the maximum transmission power of 8dBm through software configuration. Conditional users need to match RF parameters, which can improve the transmission power and is more power friendly. Increase the transmission power: the transmission power can be increased to 10db by external power supply to the van pin. If this is required, the reference circuit is as follows (0 ohm resistor is used for R3). Please consult iNGCHIPS Technology for software configuration.

