ING91683C BLE5.3 SoC Datasheet

Description

The purpose of this datasheet is to give the customers an overview of the ING91683C Bluetooth Low Energy （BLE5.3）SoC, and sufficient information for the customers integrating the SoC into a product.

The ING91683C is a Bluetooth Low Energy SoC with Bluetooth 5.3 specification compliance. It integrates INGCHIPS inhouse BLE5.3 IP including Modem, Link Layer Controller and Host. It also integrates a high performance 32bit RISC MCU with DSP and FPU, 512KB Flash, low power PMU, rich Peripherals, high performance and low power BLE RF Transceiver. The transmitter output power ranges from -27dBm to +8dBm, while receiver sensitivity is -102dBm under long range mode and -96dBm under 1M mode. The chip also supports 2.4G mode and proprietary BLE.

The ING91683C hardware and software can be tailored for different user application scenarios, such as extremely low power operation, accurate positioning, industrial or agricultural network, mesh network, home sensing and so on. The ING91683C also supports OTA and multiple boot options, allowing conveniently product feature promotion and upgrades.

Key Features

- Compliant with BLE 5.3 Specification
  - Data rate 125K/500K/1M/2M bps
  - Advertising extension
  - Frequency hopping CSA#1 and CSA#2
  - Randomized primary advertising channels
  - AoA and AoD positioning
  - Connection subrating
  - Channel classification enhancement
  - GAP, ATT/GATT, SMP, L2CAP supported
  - Link layer privacy
- Powerful Platform
  - Embedded maximum 112MHz 32bit RISC MCU with DSP and FPU, flexible cache configuation and 2-wires SWD debug interface
  - On chip 512KB Flash, ROM, 80KB RAM (with 64KB retention), 128Bit EFUSE. Supplementary external FLASH range up to 32MB
  - Support various clock sources including internal 32KHz RC and 48MHz RC oscillator, internal 500MHz PLL, and external 32.768KHz and 24MHz crystal
- Smart Power Management
  - 1.62-3.63V voltage supply
  - Integrated qualified DCDC and LDO with POR and BOR
  - Automated power management
  - Support IOs retention and wakeup
  - 0.40uA sleep with GPIO wakeup
  - 0.55uA sleep with GPIO and RTC wakeup
  - 25uA average with 500ms advertising
  - 4.5mA peak during sensitivity receving
  - 5.0mA peak during 0dBm transimitting
- Rich Peripheral Interface
  - 42 Flexible General Purpose IOs for multiple usage
  - USB2.0 full speed device support

- 2x QSPI with both master and slave mode, high speed QSPI supports 96MHz and XIP, nomal QSPI supports 24MHz
- 14-bits, 11 channels, 400ksps ADC with PGA, single-ended and differential mode
- 16 level multi-sources Comparator with wake-up function
- Programmable Peripherals Trigger Engine (PTE)
- 3x RTC
- 6x 32-bit Timers with PWM function
- 1 Watchdog
- 3x enhanced PWM with capture function
- 2x UART with flow control, support LIN
- 2x I2C with both master and slave mode
- I2S/PCM and PDM for audio
- Quadrature Decoder (QDEC)
- Hardware Key Scanner
- Embedded IR transceiver
- Mutlti-channel DMA
- 128-bit AES/CCM
- True Random Number Generator (TRNG)

■ Link Layer Features
- 128-AES/CCM Encryption/Decryption
- Link layer packet processor of types Advertising/Data/Control
- Packet processor of CRC and Whitening
- CTE in both Advertising and Connection
- All BLE events formatting and synchronization
- Extended/Periodic Advertising
- Multiple Advertising Sets (up to 1650 bytes per set)
- Multiple Connections
- All State & Role Combinations
- Privacy

■ RF and Modem Features:
- 2.200-2.600 GHz
- Sensitivity with -102dBm @125K PHY, -96dBm @1M PHY
- Output power -27dBm to +8dBm
- Frequency hopping
- Integrated PLL
- Analog RSSI with 1dBm resolution
- Automatic VCO & RX filter tuning
- Embedded Modem with programmable channel filter, AGC, DC offset cancelation, and RSSI measurement

■ Flexible Software
- Single chip solution with both application and protocol stacks
- Simple, clean and optimized API
- Configurable software to satisfy flexible application scenario. Support all device classes Broadcaster, Central, Observer, Peripheral
- Provide SDK with 50+ reference examples, such as SIG Mesh Solution, OTA example, AoA/AoD positioning, beacon, massive connection, etc.

■ Package
- QFN60: 7×7×0.75mm, pitch 0.4mm
- Operation temperature range -40° ~ 85°
- Storage temperature range -65° ~ 150°

Applications

- Indoor Positioning and Navigation
- Medical Monitoring Positioning System
- Industrial Interconnection, Data collection
- Industrial Wearables
- Smart Meter System
- Bicycle and Automobile Application
- Temperature and Humidity Collection in Agriculture and Livestock Monitoring
- Portable Devices like printers
- Fitness Equipment, Personal Wearables
- Intelligent Household
- Smart Building like Mesh Lightening
- Home Security and Alarm
- Smart Cities
- Toy control, Keyboard and Mouse, etc.
- Beacon, TV remote controller

Revision History

Version	Change Descriptions	Date	Editors
1.0.0	Initial version	16.02.2023	SoC group
1.0.1	CR 91683C.1	10.03.2023	SoC group
1.0.2	CR 91683C.2	23.05.2023	SoC group

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1 Block Diagram

The ING91683C chip is controlled by one powerful 32bit RISC MCU with FPU and DSP engine. Boot code is solidified in ROM and application code is programmed into internal or/and external Flash which are accessed through high performace inter-connect bus. Also on chip RAM and cache memory are for high speed application.

The chip is integrated with vary clock sources, low power PMU and rich Peripherals. The BLE specification is powered by high performance and low power RF Transceiver and Modem with flexible Link Layer Engine.

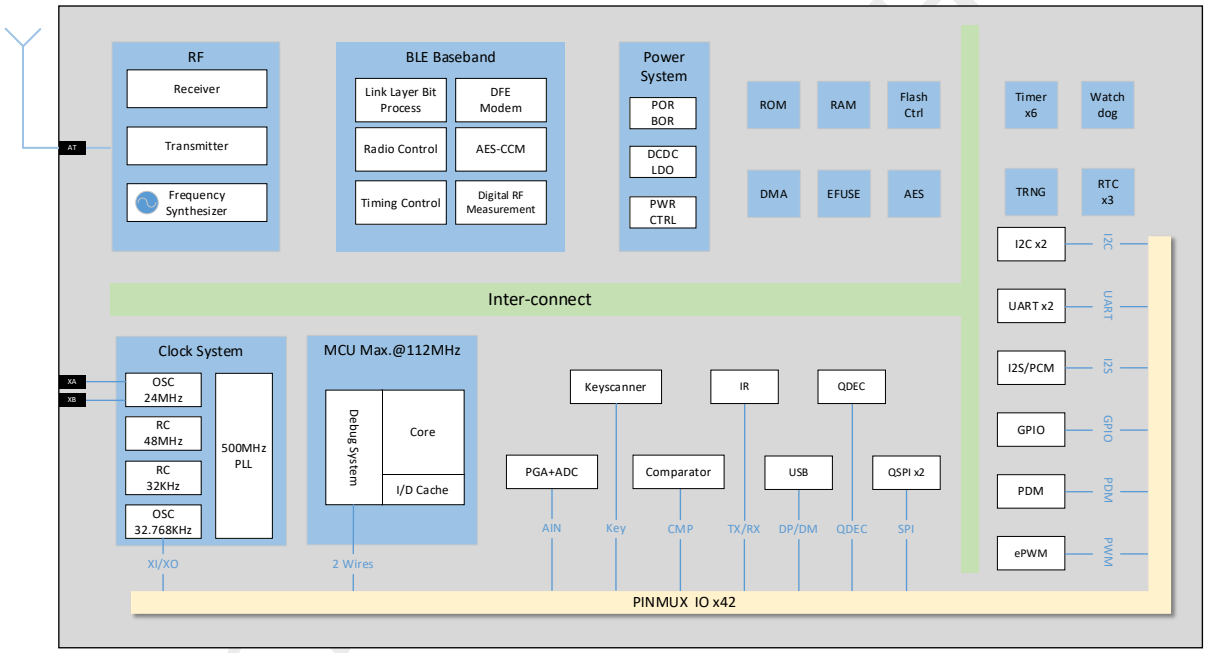


Figure 1-1 ING91683C Block Diagram

2 Main Control Blocks

2.1 Power Management

The POR-BOR in PMU is used to monitor input supply voltages which can be programmable. It is used to assert status signals indicating that the power supply voltage has crossed the specified thresholds. The POR-BOR is especially suitable on Always-On domain.

- The POR signal (for Power-On-Reset) is a single-shot signal. It is generated when the voltage crosses over a threshold.
- The BOR signal (for Brown-Out-Reset) is asserted when the voltage has dropped below a threshold. BOR is de-asserted when rising back up above the threshold plus a hysteresis.

Any load connected to the monitored power supply voltage can be enabled thanks to these status signals without risking to be trapped in undetermined states because of too low supply voltages.

The POR-BOR is autonomous, no external voltage reference or external clock are required. It includes a recovery delay circuit to minimize sensitivity to glitch during POR assertion and BOR de-assertion.

The DCDC regulator in PMU provides power for the chip, and it can be disabled when only use LDO mode. External LC filters must be connected when DCDC regulator is used. The advantage of using DCDC is that the overall power consumption is reduced as its efficiency is higher than that of LDO. In order to provide best power efficience for different applications, DCDC can switch power supply at several modes automatically.

The LDO regulator in PMU is a low dropout linear regulator which can also provides power for the chip. The LDO has excellent power supply noise rejection characteristics, which can automatically maintain the regulation of load current and stabilize the voltage output. Its output voltage can be programmable according to different applications.

2.2 Clock Controller

ING91683C has several clock sources, including Oscillator 24MHz, Oscillator 32.768KHz, RC 32KHz and RC 48MHz. One on chip PLL can also provide higher frequency clock for

complex application. Thanks to integrated clock dividers and clock switches, the clock frequencies are in wide ranges for different perpherials and applications.

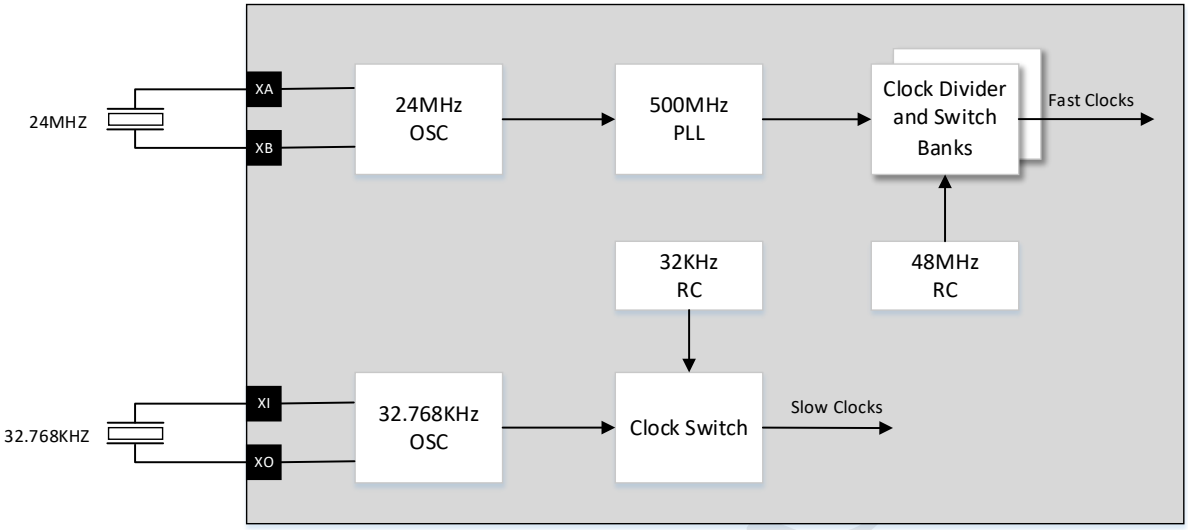


Figure 2-1 Clock Structure

2.3 Low Power Engine

In addition to the clock gating, the ING91683C chip also contains several power domains, which can automatically adapt to different working conditions and achieve excellent power consumption level.

The chip defines three power states, in each state there are also some sub-power modes for various conditions to save power.

Table 2-1 Power States

Power State	Avaiable Blocks and Wakeup Sources
Active Mode	All function blocks are available
Sleep Mode	MCU and BLE are turned off. RTC active with all or some RAM retention, wakeup by counter, comparator or IOs
Power Off	Chip is power down, wakeup by power pin

3 MCU Sub-System

3.1 Processor

The MCU processor features:

- A high performace 32-bit RISC processor core that has:
  - FPU and DSP.
  - Hardware multiplier and divider.
  - I & D caches.
  - WFI.
- Vectored interrupt controller closely integrated with the processor core to achieve low latency interrupt processing:
  - Dynamic reprioritization of interrupts.
  - Priority grouping.
  - Automatically saved on interrupt entry, and restored on interrupt exit.
  - Ultra-low power sleep mode.
- Low-cost debug solution that features:
  - Debug access to all memories and registers in the system
  - Two wire debug ports

3.2 Memory

The system contains memoris including ROM, RAM and Flash, which can be used for code and date storage.

The on chip 80KB RAM consists of 16KB RAM1(two 8KB cache shared memory) and 64KB RAM2(two 8KB and three 16KB BLE shared memory). The RAM2 also support retention function in system sleep mode.

The Flash consists of internal one (512KB) and external one. The external Flash address size can be mapped to maximum 32MB to extend the code space in XIP (eXecute In Place) mode. The system also has 128-Bit EFUSE space range to store chip and customer information.

The complete memory structure is shown in Figure 3-1.

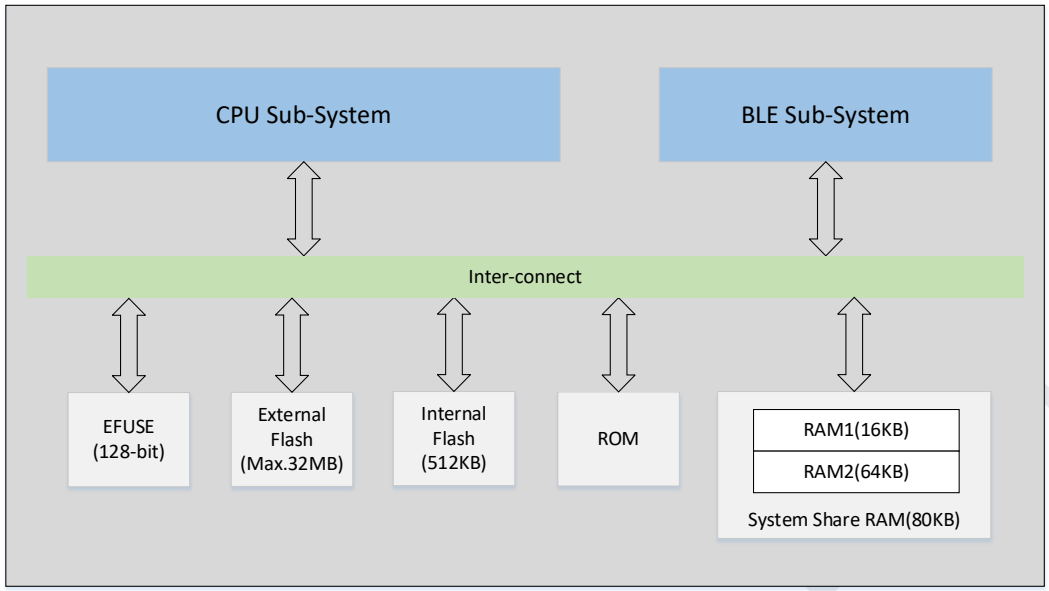


Figure 3-1 System Memory Distribution

3.3 Firmware Protection

The ING91683C supports two methods to achieve the firmware protection.

1. The bootloader-based Hardware-Lock

During the firmware burning, user can enable a Read-Protection function in downloading options to set a Hardware-Lock state into the chip.

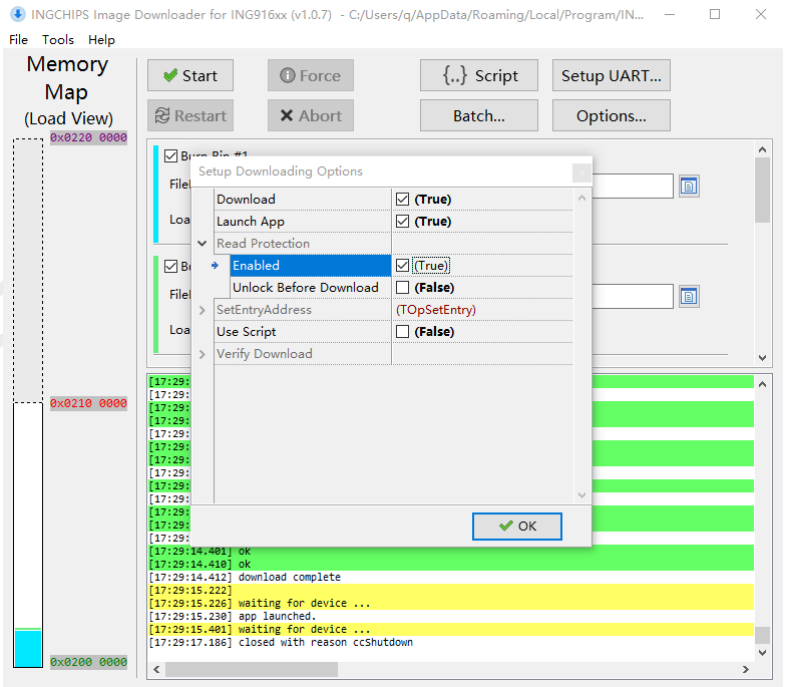


Figure 3-2 Flash Read Protection Enable Option

If the chip is in LOCK state, other firmware will not be permitted to burn into the chip. And the firmware already burned is unreadable to the third party.
If a chip in LOCK state is unlocked, the flash will be mass erased to clean the whole chip.

2. Hardware ecryption and decryption in bootloader

The firmware can be encrypted using a key generated by TRNG. If the encryption is enabled, the firmware will be encrypted when programing Flash. The data directly read from Flash will be garbled.

Together with bootloader hardware encryption, it can protect the firmware.

3.4 Peripherals

3.4.1 Pin Controller

This function block is to control the functions of all IO pins. These functions include multiplexing between all peripherals, pull-up and pull-down selection, input mode control and output drive strength control.

Features:

- Each IO pin supports multiple usage when as digital pin
- Each IO pin supports pull-up and pull-down
- Each IO pin can be configured as Schmitt input or buffer input
- Each IO pin supports 4 kinds of drive strength
- Some IO pins can be configured as digital pin or analog pin
- Most IO pins support wakeup and retention, IO18/19/20/26/27/28 can't support wakeup and retention, IO38/39/40/41 support retention function only
- IO 18/19/20/26/27/28 support high speed up to 96MHz

Each IO pin can be configued to specified function, the **Table 3-1** shows all of IO pins function mapping.

Table 3-1 IO Pins Function Mapping

Function	Signal	Mapping IO Pins Number
GPIO	gpio	0-41
SWD	swd_tck	0-17, 21, 22, 31, 34, 35
	swd_dio	0-17, 21, 22, 31, 34, 35
SPI0	spi0_clk	0-17, 19, 21, 22, 31, 34, 35
	spi0_csn	0-17, 18, 21, 22, 31, 34, 35
	spi0_miso	0-17, 21, 22, 27, 31, 34, 35
	spi0_mosi	0-17, 21, 22, 28, 31, 34, 35
	spi0_hold	0-17, 20, 21, 22, 31, 34, 35
	spi0_wp	0-17, 21, 22, 26, 31, 34, 35

SPI1	spi1_clk	0-17, 21, 22, 31, 34, 35
	spi1_csn	0-17, 21, 22, 31, 34, 35
	spi1_miso	0-17, 21, 22, 31, 34, 35
	spi1_mosi	0-17, 21, 22, 31, 34, 35
	spi1_hold	0-17, 21, 22, 31, 34, 35
	spi1_wp	0-17, 21, 22, 31, 34, 35
IR	ir_din	0-17, 21, 22, 31, 34, 35
	ir_dout	0-17, 21, 22, 31, 34, 35
I2S	i2s_lrclk	0-17, 21, 22, 31, 34, 35
	i2s_bclk	0-17, 21, 22, 31, 34, 35
	i2s_din	0-17, 21, 22, 31, 34, 35
	i2s_dout	0-17, 21, 22, 31, 34, 35
UART0	uart0_txd	0-17, 21, 22, 31, 34, 35
	uart0_rxd	0-17, 21, 22, 31, 34, 35
	uart0_rts	0-17, 21, 22, 31, 34, 35
	uart0_cts	0-17, 21, 22, 31, 34, 35
UART1	uart1_txd	0-17, 21, 22, 31, 34, 35
	uart1_rxd	0-17, 21, 22, 31, 34, 35
	uart1_rts	0-17, 21, 22, 31, 34, 35
	uart1_cts	0-17, 21, 22, 31, 34, 35
I2C0	i2c0_scl	0-17, 21, 22, 31, 34, 35
	i2c0_sda	0-17, 21, 22, 31, 34, 35
I2C1	i2c1_scl	0-17, 21, 22, 31, 34, 35
	i2c1_sda	0-17, 21, 22, 31, 34, 35
PDM	pdm_din	0-17, 21, 22, 31, 34, 35
	pdm_mclk	0-17, 21, 22, 31, 34, 35
PWM	pwm_0a	0, 2, 4, 6, 8, 10, 12, 14, 16, 21, 31, 35
	pwm_0b	1, 3, 5, 7, 9, 11, 13, 15, 17, 22, 34
	pwm_1a	0, 2, 4, 6, 8, 10, 12, 14, 16, 21, 31, 35
	pwm_1b	1, 3, 5, 7, 9, 11, 13, 15, 17, 22, 34
	pwm_2a	0, 2, 4, 6, 8, 10, 12, 14, 16, 21, 31, 35
	pwm_2b	1, 3, 5, 7, 9, 11, 13, 15, 17, 22, 34
	pwm_3a	0, 2, 4, 6, 8, 10, 12, 14, 16, 21, 31, 35
	pwm_3b	1, 3, 5, 7, 9, 11, 13, 15, 17, 22, 34
	pwm_4a	0, 2, 4, 6, 8, 10, 12, 14, 16, 21, 31, 35
	pwm_4b	1, 3, 5, 7, 9, 11, 13, 15, 17, 22, 34
	pwm_5a	0, 2, 4, 6, 8, 10, 12, 14, 16, 21, 31, 35
	pwm_5b	1, 3, 5, 7, 9, 11, 13, 15, 17, 22, 34
	pwm_6a	0, 2, 4, 6, 8, 10, 12, 14, 16, 21, 31, 35
	pwm_6b	1, 3, 5, 7, 9, 11, 13, 15, 17, 22, 34
	pwm_7a	0, 2, 4, 6, 8, 10, 12, 14, 16, 21, 31, 35
	pwm_7b	1, 3, 5, 7, 9, 11, 13, 15, 17, 22, 34
	pwm_8a	0, 2, 4, 6, 8, 10, 12, 14, 16, 21, 31, 35
	pwm_8b	1, 3, 5, 7, 9, 11, 13, 15, 17, 22, 34
	cap_in0	0-17, 21, 22, 31, 34, 35
	cap_in1	0-17, 21, 22, 31, 34, 35
	cap_in2	0-17, 21, 22, 31, 34, 35
	cap_in3	0-17, 21, 22, 31, 34, 35
	cap_in4	0-17, 21, 22, 31, 34, 35
	cap_in5	0-17, 21, 22, 31, 34, 35
BLE	ant_sw0	0, 3, 6, 9, 12, 15, 21, 34
	ant_sw1	1, 4, 7, 10, 13, 16, 22, 35
	ant_sw2	2, 5, 8, 11, 14, 17, 31
	ant_sw3	0, 3, 6, 9, 12, 15, 21, 34
	ant_sw4	1, 4, 7, 10, 13, 16, 22, 35
	ant_sw5	2, 5, 8, 11, 14, 17, 31
	ant_sw6	0, 3, 6, 9, 12, 15, 21, 34

	ant_sw7	1, 4, 7, 10, 13, 16, 22, 35
	pa_txen	4-10, 34, 35
	pa_rxen	11-17, 34, 35
Key Scanner	key_row	0-17, 21-25, 29-41
	key_col	0-17, 21-25, 29-41
QDEC	qdec_phasea	0-17, 21, 22, 31, 34, 35
	qdec_phaseb	0-17, 21, 22, 31, 34, 35
	qdec_index	0-17, 21, 22, 31, 34, 35
32.768KHz Crystal	XI	5
	XO	6
USB	DP	16
	DM	17
ADC	AIN	7, 8 ,9 ,10, 11, 12, 13, 14, 30, 31, 35
Comparator	VINP	1, 2, 4, 18, 20, 26, 27, 28
	VINN	3, 15, 19

3.4.2 GPIO

The General Purpose Input/Output (GPIO) function block is usually used to driving LEDs or other indicators, controlling off-chip devices, sensing digital inputs, detecting edges, and bringing the part out of power-down mode. The ING91683C has 42 GPIOs that could be assigned to IO Pins via the Pin Controller. The mapping table is shown in Table 3-2.

Features:

- Each individual GPIO pin can be configured as input or output.
- Each individual GPIO pin can serve as an interrupt request.
- Interrupts can be configured on single positive or negative edges, or on both edges, or on high level or low level
- Hardwre input de-bounce

Table 3-2 GPIO Mapping Table

Pin Name	GPIO	Pin Name	GPIO	Pin Name	GPIO	Pin Name	GPIO
IO0	GPIO[0]	IO11	GPIO[11]	IO22	GPIO[22]	IO33	GPIO[33]
IO1	GPIO[1]	IO12	GPIO[12]	IO23	GPIO[23]	IO34	GPIO[34]
IO2	GPIO[2]	IO13	GPIO[13]	IO24	GPIO[24]	IO35	GPIO[35]
IO3	GPIO[3]	IO14	GPIO[14]	IO25	GPIO[25]	IO36	GPIO[36]
IO4	GPIO[4]	IO15	GPIO[15]	IO26	GPIO[26]	IO37	GPIO[37]
IO5	GPIO[5]	IO16	GPIO[16]	IO27	GPIO[27]	IO38	GPIO[38]
IO6	GPIO[6]	IO17	GPIO[17]	IO28	GPIO[28]	IO39	GPIO[39]
IO7	GPIO[7]	IO18	GPIO[18]	IO29	GPIO[29]	IO40	GPIO[40]
IO8	GPIO[8]	IO19	GPIO[19]	IO30	GPIO[30]	IO41	GPIO[41]
IO9	GPIO[9]	IO20	GPIO[20]	IO31	GPIO[31]		
IO10	GPIO[10]	IO21	GPIO[21]	IO32	GPIO[32]		

3.4.3 UART

There are two separate UART function blocks in the chip. The UART performs serial-to-parallel conversion on data received and parallel-to-serial conversion on data transmitted.The CPU/DMA reads and writes data and control/status information of UART through the inter-connect bus. The transmit and receive paths are buffered with internal FIFO memories enabling up to 32-bytes to be stored independently in both transmit and receive modes.

Features:

- Support LIN with both master and slave mode
- Hardware flow control
- A programmable baud rate generator, up to 7000000bps
- Independent transmit and receive FIFO
- Individually-maskable interrupts from the receive (including timeout), transmit, modem status and error conditions
- A single combined interrupt so that the output is asserted if any of the individual interrupts are asserted, and unmasked
- DMA supported

UART timing diagram is as below:

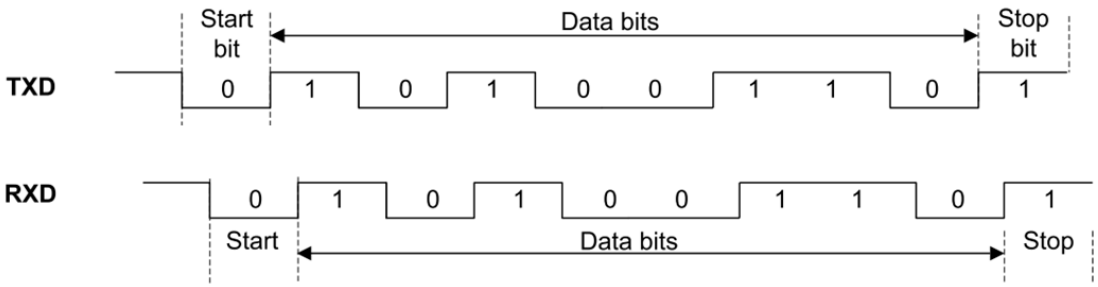


Figure 3-3 UART Timing Diagram

3.4.4 I2C

There are two separate I2C function blocks in the chip. The I2C is a standard two-wire serial interface used to connect the chip with peripherals or host controllers. This interface provides a standard speed (up to 100 kbps), and a fast speed (up to 400 kbps) I2C connection to multiple devices with the chip acting in either I2C master mode or I2C slave mode.

Features:

- Programmable as a master device or slave device
- Supports standard speed up to 100kbps, fast speed up to 400kbps
- Pogrammable 7-bit and 10-bit device addresses

- Shared RX and TX FIFO
- Programble clock and data timing
- DMA supported

The I2C timing diagram is as below:

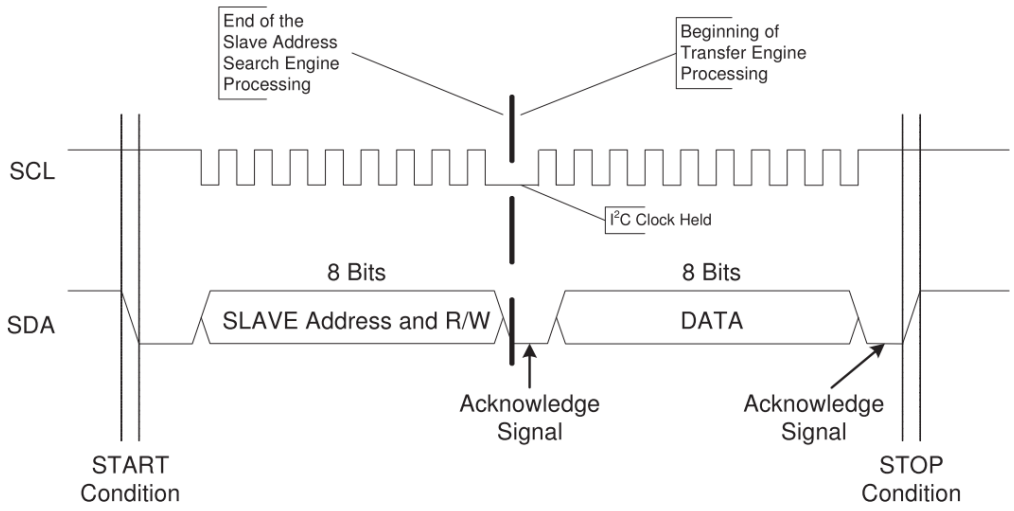


Figure 3-4 I2C Timing Diagram

3.4.5 QSPI

There are two separate QSPI function blocks (SPI0 and SPI1) in the chip with qural mode. Both SPI0 and SPI1 support master and slave mode, SPI0 also supports external Flash XIP in quad mode.

SPI0 features:

- XIP (eXecute In Place) supported to extend flash space with max. 96MHz clock frequency
- Max. 96MHz clock frequency in master mode, max. 24MHz in slave mode
- Programmable master and slave mode
- Separate transmit and receive FIFO
- Configurable single, dual and qurad modes
- Configurable clock polarity and phase
- DMA supported

SPI1 features:

- Max. 24MHz clock frequency in master and slave mode
- Programmable master and slave mode
- Separate transmit and receive FIFO

- Configurable single, dual and qurad modes
- Configurable clock polarity and phase
- DMA supported

The SPI timing diagrams are as below:

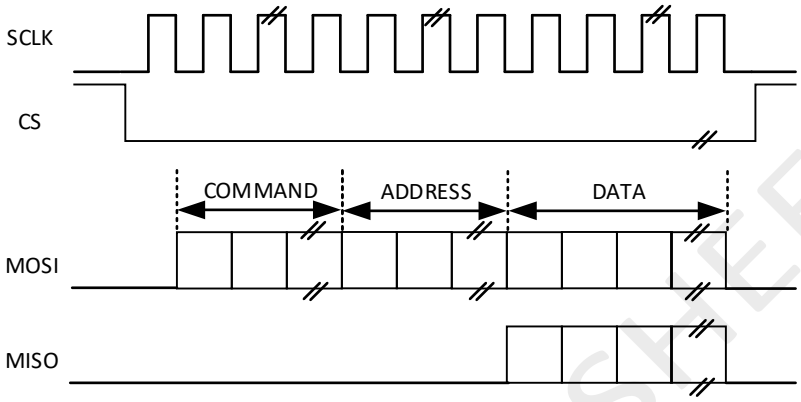


Figure 3-5 SPI Master Timing Example

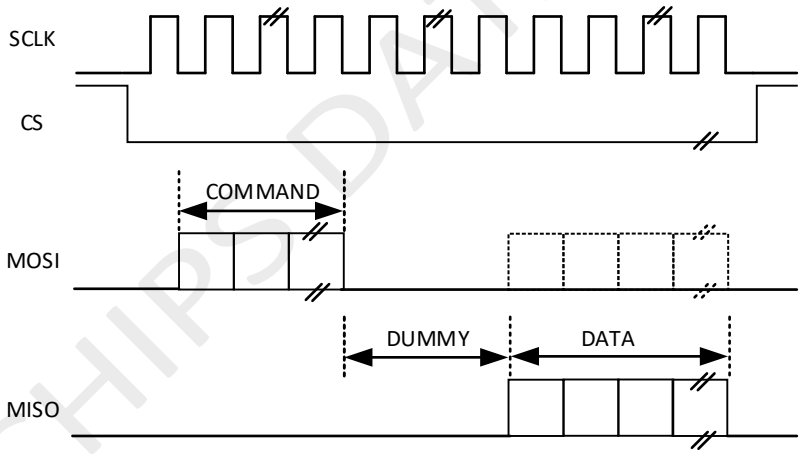


Figure 3-6 SPI Slave Timing Example

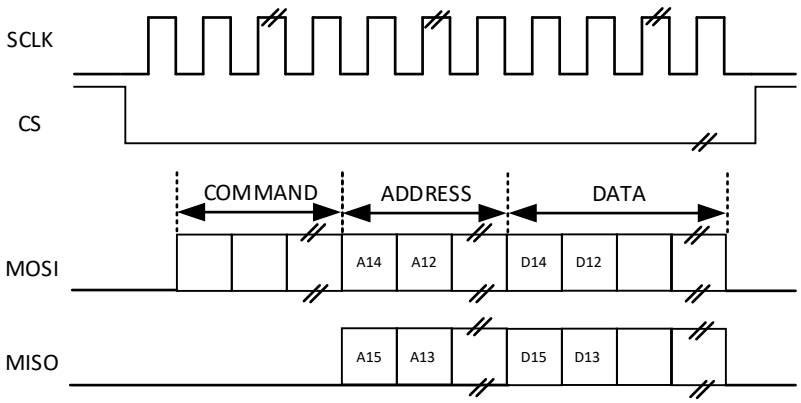


Figure 3-7 SPI Dual Mode Timing Example

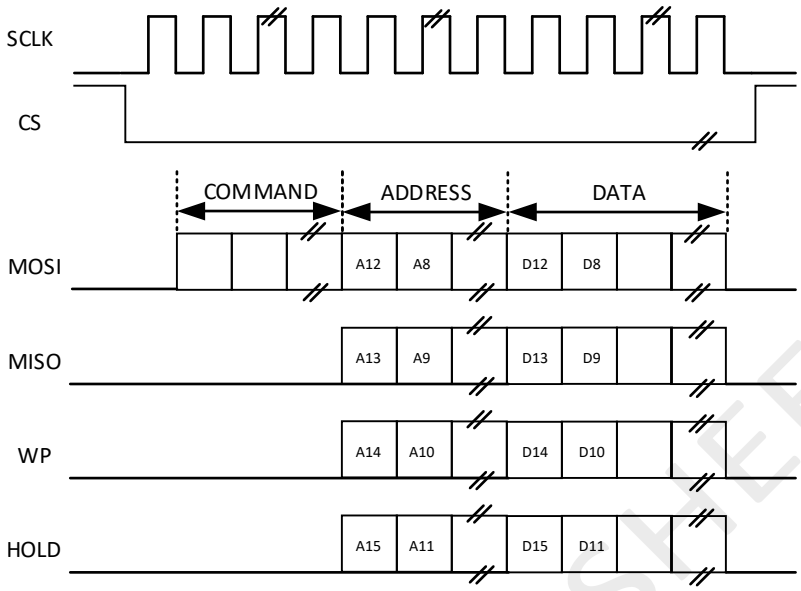


Figure 3-8 SPI Quad Mode Timing Example

3.4.6 USB

The ING91683C has a full-speed (12 Mbps) USB interface for communicating with other compatible digital devices. The USB interface acts as a USB peripheral, responding to requests from a master host controller. The chip contains internal 1.5 kOhm pull up resistor for the DP pin.

Features:

- Implements full-speed (12 Mbps) device fully compliant to Universal Serial Bus Specification Revision 2.0
- Integrated USB PHY
- Software controlled on-chip pull-up on DP
- Supports USB suspend
- Independent DMA
- Supports DP and DM pin multiplex with other peripherals

3.4.7 I2S with PCM

I2S bus is a special bus for digital audio. It has four pins, two data pins (DOUTand DIN), one bit rate clock pin (BCLK) and one left and right channel selection pin (LRCLK). In addition, with the output of MCLK from the ING91683C, it can be used to provide clock for external DAC/ADC chip

Features:

- Support I2S standard mode and left alignment mode
- Support PCM (Pulse Code Modulation) timing
- Programmable master and slave mode
- Configurable LRCLK and BCLK polarity
- Configurable data bit width
- Independent transmit and receive FIFO
- Support Stereo and Mono mode
- Configurable sampling frequency
- DMA supported

The I2S timing diagrams are as below:

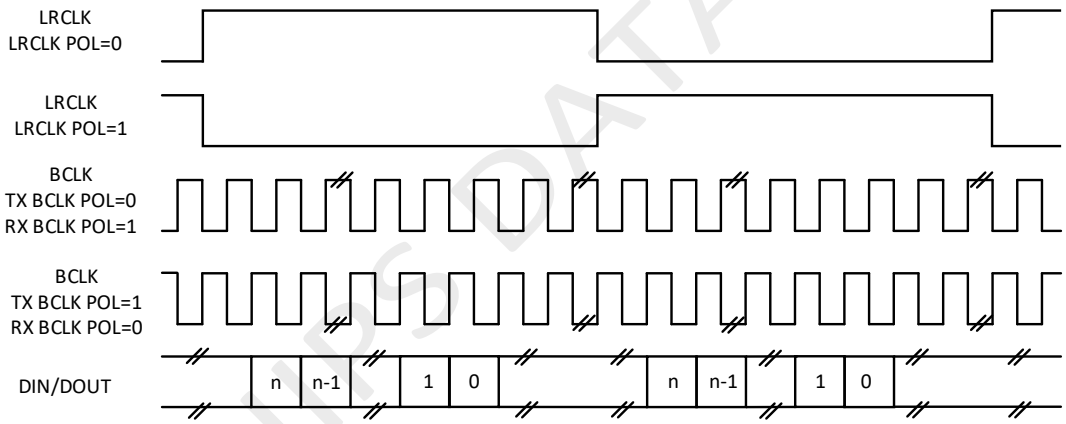


Figure 3-9 I2S Standard Mode

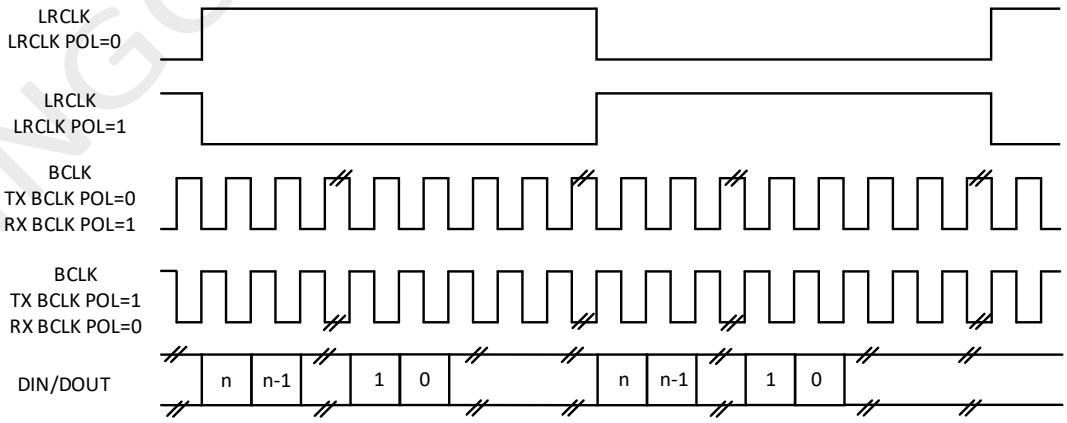


Figure 3-10 I2S Left Alignment Mode

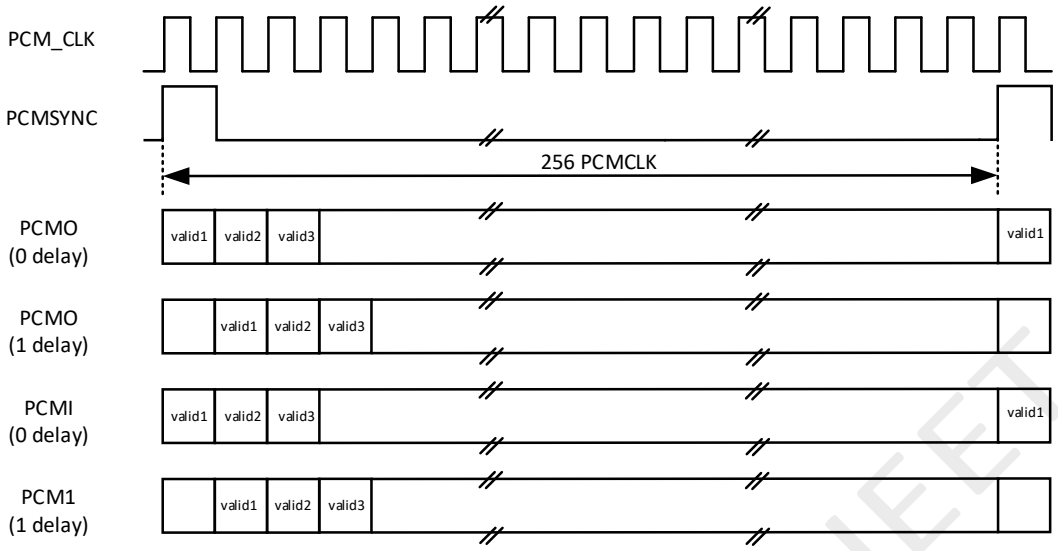


Figure 3-11 PCM Mode

3.4.8 PDM

The pulse density modulation (PDM) function block handles input of pulse density modulated signals from external audio frontends like digital microphones. This block generates the PDM clock and supports dual-channel (Left and Right) data input.

Features:

- Supports dual-channel with the same data input
- Multi-sample rate, 24-bit data width
- HW decimation filters
- DMA and I2S supported for sample buffering

3.4.9 PTE

The peripheral trigger engine (PTE) function block has programmable internal connections within different peripherals, which enable peripherals to interact autonomously with each other. The PTE allows precise synchronization between peripherals when real-time application constraints exist and eliminates the need for CPU activity to implement behavior which can be predefined using PTE.

Features:

- 4 channels
- Up to 24 sources and 24 destinaions
- Programmable channel enable

- Programmable source and destination mask

3.4.10 QDEC

QDEC can decode the signals for the PhaseA and PhaseB of external device, reporting step count and direction.

Features:

- Configurable sample rate
- Configurable interrupt timer
- Support de-bounce filter
- 16 bits counter
- Support DMA

The outside quadrature encoder is an incremental motion encoder as which outputting two waveforms, PhaseA and PhaseB. The two inputs of QDEC waveforms are always 90 degrees out of phase, meaning that one always changes level before the other. The direction of movement is indicated by which of these two waveforms that changes level first.

The index of QDEC is controlled by register and has two sources: from GPIO or from internal driver. At the end of the event which is controlled by index, a DMA request will be triggered and the result will be loaded to the counter which can be read out from inter-connect bus. If detecting clockwise waveform, it will increase, otherwise it will reduce.

The QDEC supports de-bounce filter. The PhaseA and PhaseB must keep stable within the filter period, and then pass through to the decoder.

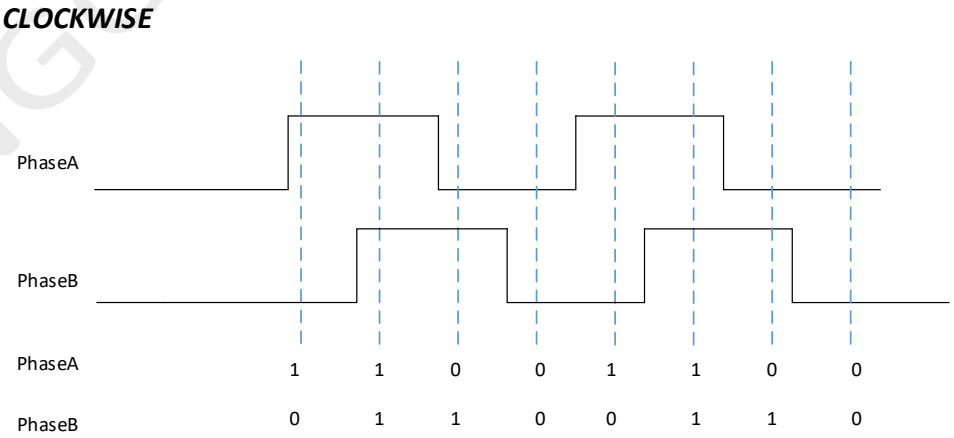


Figure 3-12 QDEC Clockwise

ANTICLOCKWISE

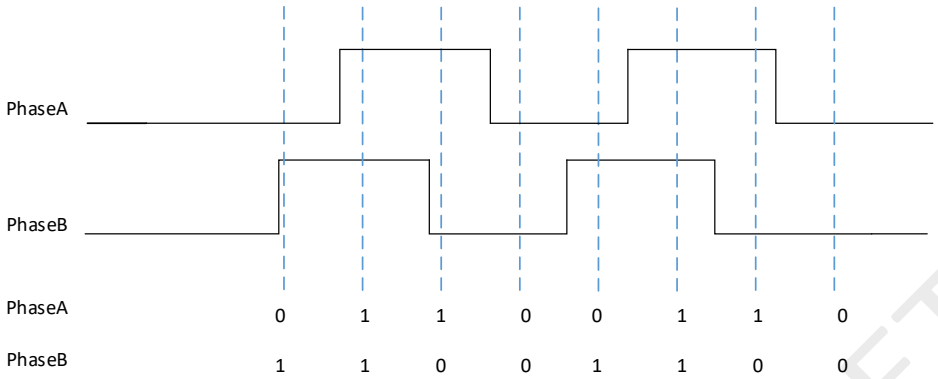


Figure 3-13 QDEC Anti-Clockwise

3.4.11 Hardware KeyScanner

Key-scanner supports scan matrix up to 18 rows * 18 columns, or 16 rows * 20 columns, or 20 rows * 16 columns. Each individual rows or columns can be enabled or disabled through register settings. De-bounce time, scan interval and release time can be configured by registers. Key-scanner supports multi key press.

A valid key press can trigger an interrupt when key-scanner interrupt is enabled.

Features:

- Configurable matrix (max.18*18 or 16*20 or 20*16)
- Configurable clock
- Support input de-bounce
- Support interval configuration
- Support DMA

3.4.12 IR

The IR function block provides a flexible way of transimitting and receiving IR code used in remote controllers. It could send IR wavefrom within IR carrier and received IR waveform within IR carrier.

Features:

- Programmable transimitting carrier frequency and duty
- Hardware transimitting waveform control
- Programmable sample clock
- Ability to learn IR waveform directly

3.4.13 DMA

The ING91683C integrates one direct memory access controller, it can transfer data efficiently between devices of the chip.

Features:

- Support 8 channles
- Support 21 request/acknowledge pairs for hardware handshake
- Support of group round-robin arbitration scheme with 2 priority levels
- Support of chain transfers
- Support 8/16/32-bit wide data transfers

3.4.14 Enhanced PWM

The PWM function block can be configured to PWM (pulse width modulation) mode or PCM (pulse capture module) mode. The PWM mode enables the generation of pulse width modulated signal to controls the external components. The PCM mode can capture the input edges.

Features:

- Support 3 channels PWM, each channel generates two PWM out
- Each PWM channel can be controlled by register or PWM sequence
- Each channel can be masked
- Support multiple modes: command mode, single step mode, symmetric mode, dead zone mode
- Support DMA to update configuration to PWM
- Support 3 channels PCM, each channel supports two PCM input
- Support both edges capture by PCM
- Support DMA for PCM

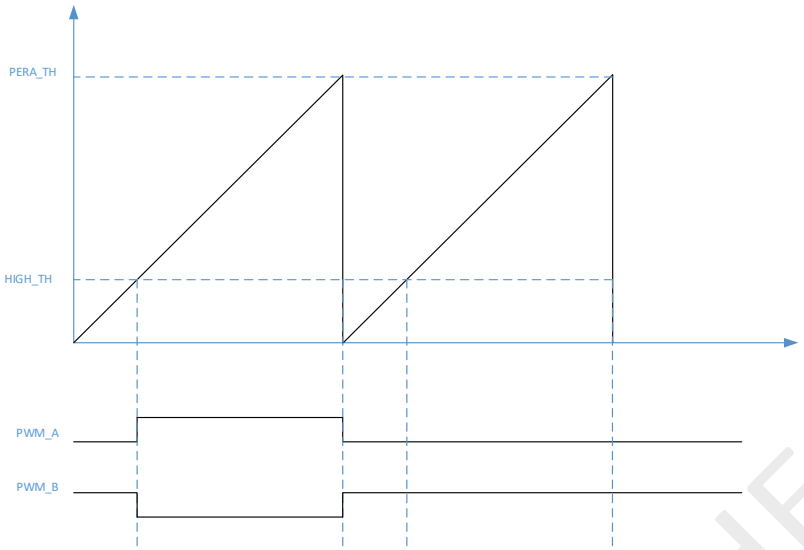


Figure 3-14 PWM Single Step Mode

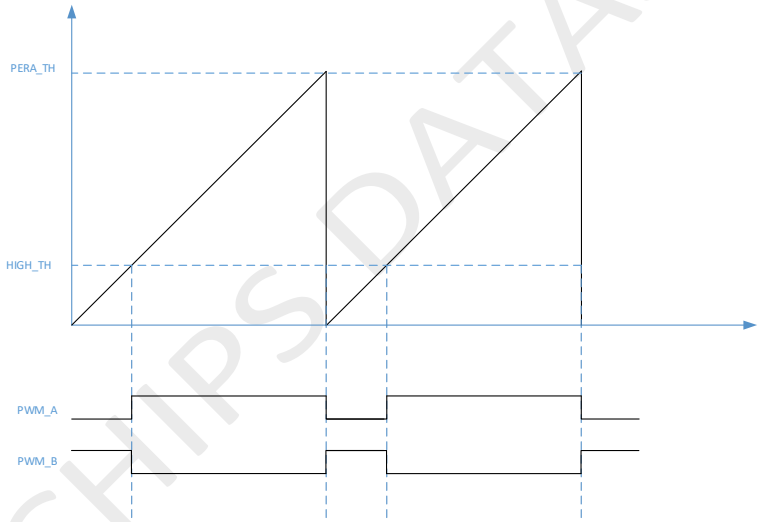


Figure 3-15 PWM Up Without Died-zone Mode

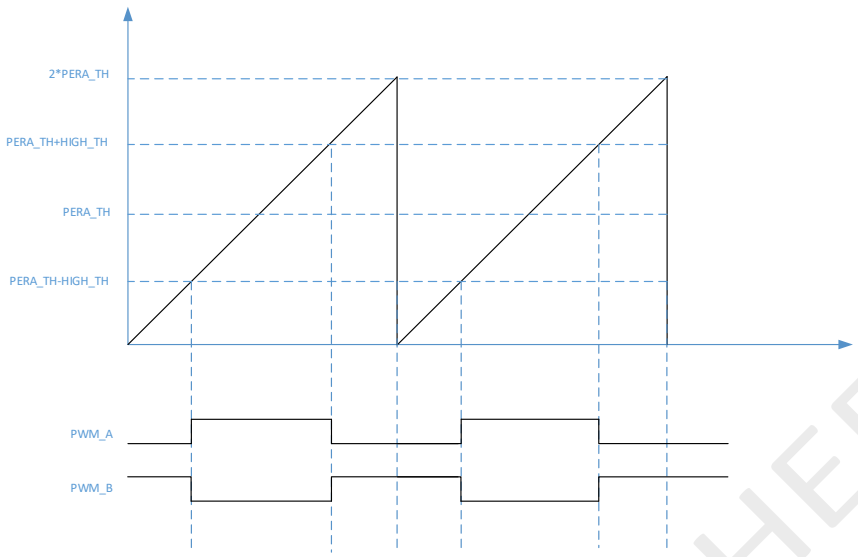


Figure 3-16 PWM Up-down Without Died-zone Mode

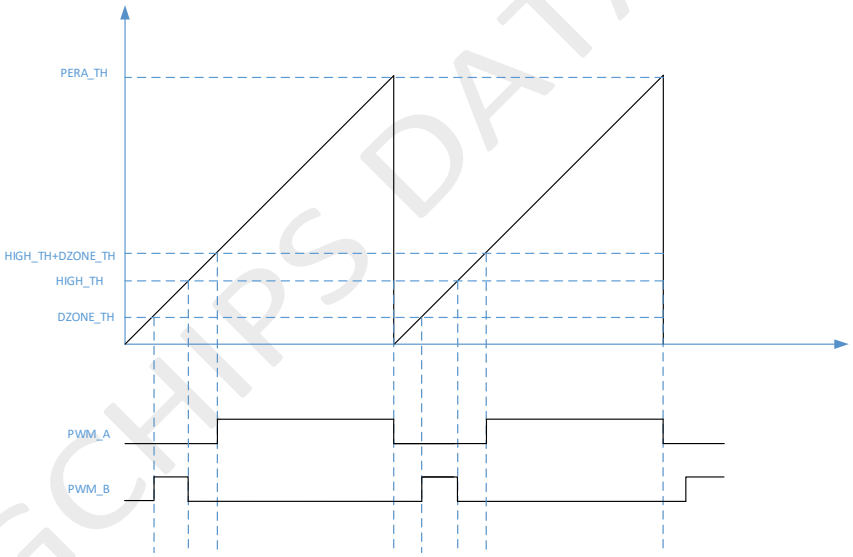


Figure 3-17 PWM Up With Died-zone Mode

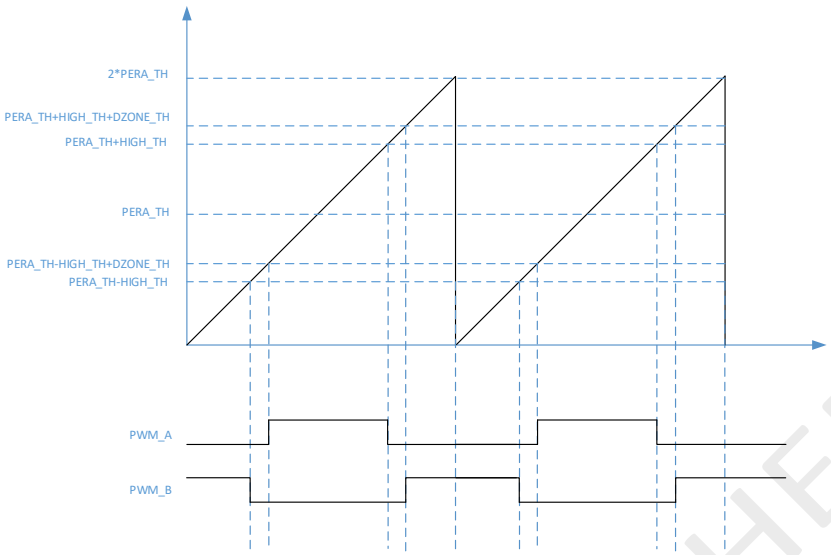


Figure 3-18 PWM Up-down With Died-zone Mode

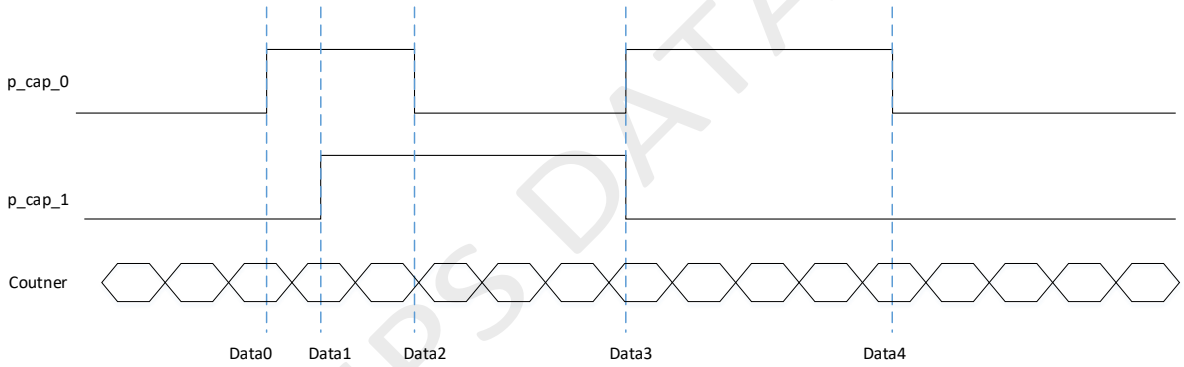


Figure 3-19 Pulse Capture Module

3.4.15 Timer with PWM

The chip has 3 timers, they are function identical. Each timer has 2 channels, each channel has a 32-bit timer. So there are six 32-bit timers in the chip. Each of the timer can also be used as PWM generator or simple timers.

Features:

- Each timer has 2 channels, each channel has a 32-bit timer
- Each channel can be programable to two 16-bit timers or four 8-bit timers
- Each channel can be programable to one PWM and generates two PWM out
- Programmable source of timer clock
- Timers can be paused

3.4.16 Watchdog

The watchdog function provides a way of recovering from software crashes.

Features:

- Both interrupt and reset generation
- Write protection mechanism
- Programmable source of timer clock
- Watchdog timer can be paused

3.4.17 RTC

There are three RTC function blocks in the chip: RTC0, RTC1 and RTC2. RTC0 keeps track of current time information and provides periodic and alarm interrupts. RTC1 maintains the BLE base time slot counters when chip sleep. RTC2 is a free running counter all the time when the chip is powered. All the RTC can wakeup the chip from sleep.

RTC0 Features:

- Configurable counter size
- Periodic interrupts: half-second, second, minute, hour and day
- Programmable alarm interrupt

RTC1 Features:

- Maintains the BLE base time slot counters when the chip is in sleep
- Automatic trimming to compensate for inaccuracies of low power clock
- Programmble trimming time

RTC2 Features:

- Free running
- Support 8 years counting

3.4.18 Comparator

The comparator (CMP) compares two input voltages to get output high or low level accordingly. One input named VINP can be derived from an analog input pin, the other input named VINN can be derived from another analog input pin or internal source as reference.

Features:

- Supports rail-to-rail input

- Supports 4 kinds of power consumption modes, ultra-low power mode, low power mode, middle power mode and high power mode
- Exactly deal low to 20mV differential voltage
- Supports hysteresis voltage
- Supports 8 channels VINP, 6 channels VINN of which one channel is in chip
- Multiple reference source with 16-levels reference ladder

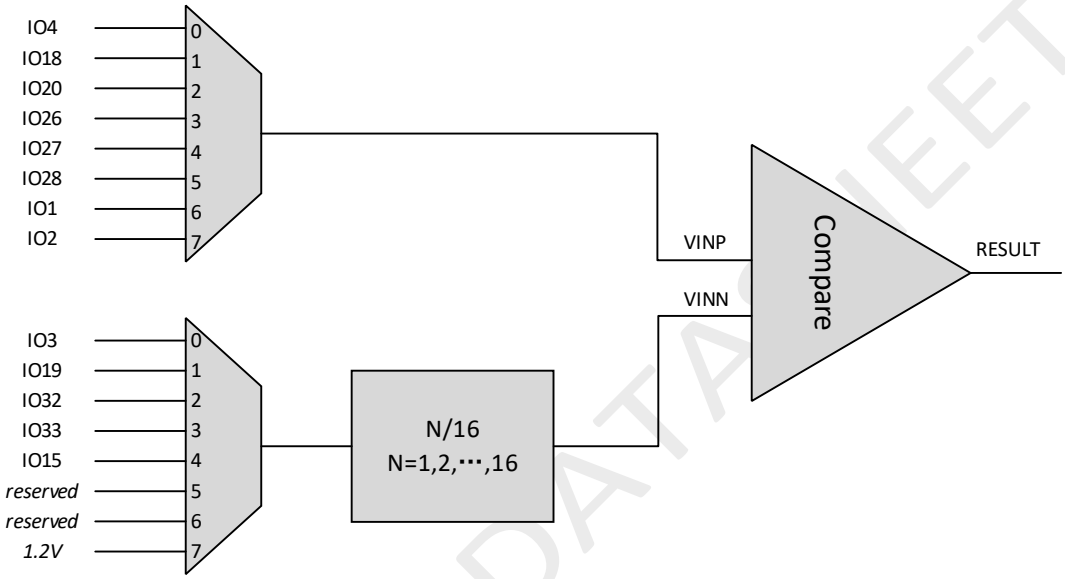


Figure 3-20 Comparator overview

3.4.19 **ADC**

The ADC (Analog-to-Digital Converter) function block can be used to measure voltage through IO Pins.

Features:

- Up to 11 single-end input channels or 4 differential input channels.
- 14-bit resolution, 1Ksps~400Ksps sampling rate range
- Support PGA
- Support single conversion mode
- Support loop conversion mode, each channel can be enabled or disabled

Table 3-3 ADC Single-end and Differential Input Mapping

Differential Input	Single-end Input	IO Pin
AIN0/AIN1	AIN0	IO7
	AIN1	IO8
AIN2/AIN3	AIN2	IO9
	AIN3	IO10
AIN4/AIN5	AIN4	IO11
	AIN5	IO12
AIN6/AIN7	AIN6	IO13
	AIN7	IO14
N/A	AIN8	IO35
N/A	AIN10	IO30
N/A	AIN11	IO31

3.4.20 **AES**

The ING91683C embeds hardware engine to support 128-AES encryption and decryption. There are two methods to perform encryption and decryption operations, one is software mode that the firmware starts the engine to work, the other is hardware mode that BLE Core starts the engine to work automatically during packets processing.

The AES operation will be described using the sample data from BLE specification as below,

```
Key (16-octet value MSO to LSO): 0x4C68384139F574D836BCF34E9DFB01BF
Plaintext_Data (16-octet value MSO to LSO): 0x0213243546576879acbdcedfe0f10213
Encrypted_Data (16-octet value MSO to LSO): 0x99ad1b5226a37e3e058e3b8e27c2c666


The Key is LTK.
The Plaintext Data is SKD = SKDm || SKDs
SKDm = 0xACBDCEDFE0F10213 (MSO to LSO)
SKDs = 0x0213243546576879 (MSO to LSO)
SKDm is put in the LSB
```

Before start the hardware engine, the four registers will store the LTK as Little-endian format:

Table 3-4 LTK Data Format

Bits	[31:24]	[23:16]	[15:8]	[7:0]
Register KEY0	0x9D	0xFB	0x01	0xBF
Register KEY1	0x36	0xBC	0xF3	0x4E
Register KEY2	0x39	0xF5	0x74	0xD8
Register KEY3	0x4C	0x68	0x38	0x41

When start AES operation, the input data are put in memory occupying four continuous addresses. For example, the four memory addresses will store the input data SKD as Little-endian format.

Table 3-5 SKD Data Format

Bit	[31:24]	[23:16]	[15:8]	[7:0]
Memory Addr0	0xe0	0xf1	0x02	0x13
Memory Addr1	0xac	0xbd	0xce	0xdf
Memory Addr2	0x46	0x57	0x68	0x79
Memory Addr3	0x02	0x13	0x24	0x35

After AES operation, the output encrypted data is Big-endian format.

Table 3-6 Encrypted Data Format

Bit	[31:24]	[23:16]	[15:8]	[7:0]
Memory Addr4	0x52	0x1b	0xad	0x99
Memory Addr5	0x3e	0x7e	0xa3	0x26
Memory Addr6	0x8e	0x3b	0x8e	0x05
Memory Addr7	0x66	0xc6	0xc2	0x27

3.4.21 TRNG

The true random number generator (TRNG) generates true random numbers based on internal thermal noise that are suitable for cryptographic purpose, which does not require a seed value.

Features:

- Configurable generation rate
- Pseudo random operation to average the 0 and 1 in the random number
- Support single mode or continuous mode

4 BLE5.3 Sub-System

4.1 RF Transceiver

The radio provides best in class RX and TX metrics at highly optimized area and current. It supports 1Mbps, 2Mbps and Long Range (125Kbps and 500Kbps), it is compliant with BLE 5.3. The RF consists of the RX chain from LNA to ADC, the TX chain from DAC to TX PA, the synthesizer subsystem that generates the LO frequency and LDOs. The transceiver specifications are listed in Table 4-1 and Table 4-2.

4.1.1 Transmitter Specification

Table 4-1 Transmitter Specification

Parameters	Min.	Typ.	Max.	Unit	Conditions
Output Power	-27	0	+8	dBm	
1Mbps Mode					
In Band Emissions (2/3 MHz Offset)		-57/-58		dBm	Typical gain setting
Out Band Emissions (2^{nd}/3^{rd} Harmonic)		-53/-53		dBm	Typical gain setting
2Mbps Mode					
In Band Emissions (4/5/6 MHz Offset)		-59/-60 /-61		dBm	Typical gain setting
Out Band Emissions (2^{nd}/3^{rd} Harmonic)		-53/-53		dBm	Typical gain setting
500Kbps LR Mode					
In Band Emissions (2/3 MHz Offset)		-57/-58		dBm	Typical gain setting
Out Band Emissions (2^{nd}/3^{rd} Harmonic)		-53/-53		dBm	Typical gain setting
125Kbps LR Mode					
In Band Emissions (2/3 MHz Offset)		-57/-58		dBm	Typical gain setting
Out Band Emissions (2^{nd}/3^{rd} Harmonic)		-53/-53		dBm	Typical gain setting

4.1.2 Receiver Specification

Table 4-2 Receiver Specification

Parameters	Min.	Typ.	Max.	Unit	Conditions
1Mbps Mode					
Receiver Sensitivity			-96	dBm	
Usable RX Signal			6	dBm	
Co-channel Interference (C/I)		9		dB	Desired Signal @ -67dBm
Image Interference (C/I)		-28		dB	Desired Signal @ -67dBm
2Mbps Mode					
Receiver Sensitivity			-93	dBm	
Usable RX Signal			6	dBm	
Co-channel Interference (C/I)		9		dB	Desired Signal @ -67dBm

Image Interference (C/I)		-28		dB	Desired Signal @ -67dBm
500Kbps LR Mode					
Receiver Sensitivity			-98	dBm	
Usable RX Signal			6	dBm	
Co-channel Interference (C/I)		5		dB	Desired Signal @ -72dBm
Image Interference (C/I)		-31		dB	Desired Signal @ -72dBm
125Kbps LR Mode					
Receiver Sensitivity			-102	dBm	
Usable RX Signal			6	dBm	
Co-channel Interference (C/I)		3		dB	Desired Signal @ -79dBm
Image Interference (C/I)		-32		dB	Desired Signal @ -79dBm

4.2 BLE Core

The BLE core includes modem, link layer and protocol controller, which supports the features required by Bluetooth 5.3. It provides qualified features as below:

- Support data rate 1Mbps, 2Mbps, 125Kbps and 500Kbps
- Support accurate RSSI indication with resolution 1dB
- Support modulation and demodulation, calibration for radio optimization
- Support BLE AoA transimit and receive with 1 us and 2 us switching and sampling slots
- Support BLE AoD transimit and receive with 1 us and 2 us switching and sampling slots
- Support proprietary AoA and AoD transimit and receive
- Support antenna switching pattern length up to 75
- Support advertising extension
- Support 128-AES/CCM Encryption/Decryption,
- Support link layer packet types Advertising/ Data/Control
- Support packet processing of CRC and Whitening
- Support Preamble and Access Address Detection
- Support Frequency Hopping CSA#1 and CSA#2
- Support random primary advertising
- Support White List searching
- Support Resolving List searching and generation
- Support all BLE events formatting and synchronization
- Support all device classes (Broadcaster, Central, Observer, Peripheral)
- Support connection in sleep mode

5 Electrical Specifications

5.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

Characteristiscs	Symbol	Min.	Max.	Unit	Notes
Supply voltage	VDD	-0.3	3.63	V	
ESD HBM	ESD_{HBM}		3000	V	Follow JEDEC EIA/JESD22-A114, Zap 3 Pulses
ESD CDM	ESD_{CDM}		1000	V	Flollow JEDEC EIA/JESD22-C101
Storage temperature	$Store_{Temp}$	-65	+150	°C	
Flash endurance	NVM_{Cyc}	100,000		Cycles	Pgrogram/Erase
Flash rention	NVM_{Ret}	20		Years	

5.2 Recommended Operating Conditions

Table 5-2 Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating temperature	T_J	-40	25	85	°C	
Supply voltage	VDD	1.62	3.3	3.63	V	
Serial clock frequency	$Clock_{spi}$			96	MHz	
	$Clock_{i2c}$			1	MHz	

5.3 DC Charateristics

Table 5-3 DC Charateristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
TX current	I_{TX}		5.0		mA	At 0dBm output, 3.3V
RX current	I_{RX}		4.5		mA	At sensitivity level, 3.3V
Sleep 1 current	I_{Sleep1}		0.4		uA	With GPIO wakeup
Sleep 2 current	I_{Sleep2}		0.55		uA	With GPIO and RTC wakeup
Sleep 3 current	I_{Sleep3}		1.4		uA	With GPIO and RTC wakeup, 16KB RAM retention
Sleep 4 current	I_{Sleep4}		4.4		uA	With GPIO and RTC wakeup, BLE maintained, 64KB RAM retention

5.4 AC Charateristics

5.4.1 External 32.768KHz Crystal Oscillator

Table 5-4 32.768KHz Crystal Oscillator Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Nominal frequency	F_{X32K}		32.768		KHz	
Frequency accuracy	F_{ACC_X32K}	-50		+50	ppm	Can be calibrated for low power
Load capacitance	$C_{L\ X32K}$	4		7	pF	
Equivalent resistance	ESR_{X32K}		35	80	ohm	

The two XO pins can be configured as two GPIO pins if the external crystal is not used.

5.4.2 Internal 32KHz RC Oscillator

Table 5-5 32KHz RC Oscillator Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Nominal frequency	F_{RC32K}		32		KHz	
Frequency accuracy	F_{ACC_RC32K}			3%	-	Can be calibrated in sleep mode

5.4.3 External 24MHz Crystal Oscillator

Table 5-6 24MHz Crystal Oscillator Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Nominal frequency	F_{X24M}		24		MHz	
Frequency accuracy	F_{ACC_X24M}	-20		+20	ppm	Frequency accuracy depends on XTAL Spec.
Load capacitance	$C_{L\ X24M}$	7.5		10	pF	
Equivalent resistance	ESR_{X24M}			60	ohm	

To reducing the BOM cost, the ING91683C has the internal build-in capacitor to replace the external capacitor. In order for this, the load capacitance of the crystal is recommended to be in the range of 7.5pF to 10pF. If customer uses different values of the load capacitance, please contact Ingchips.

5.4.4 Internal 48MHz RC Oscillator

Table 5-7 48MHz RC Oscillator Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Nominal frequency	F_{RC24M}	8	24	48	MHz	
Frequency accuracy	$F_{ACC\ RC24M}$		0.3%		-	Typical at 25°C
Stable time	$T_{OST\ RC24M}$			10	us	

The programmable output frequency: 8MHz/16MHz/24MHz/32MHz/48MHz

5.4.5 Internal PLL

The ING91683C integrates one ultra-low power PLL which can generate independent clock frequencies from 1MHz to 500MHz. It intends for the application that needs high system clocks frequency to get high performance.

Table 5-8 PLL Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Nominal frequency	F_{PLL}	1	100	500	MHz	
Stable time	T_{PLL}			120	us	

5.4.6 ADC

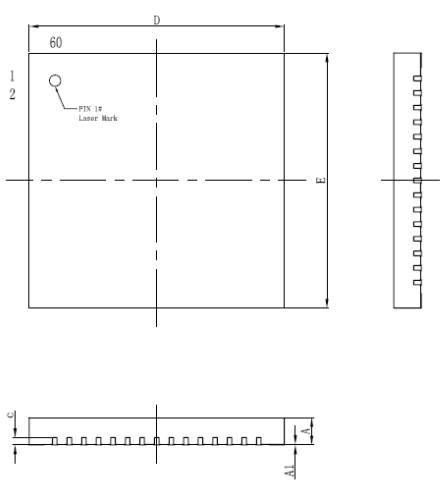
Table 5-9 ADC Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
ADC resolution	R_{adc}		14		bit	
Input full scale range	FSR_{adc}	0		VREFP	V	VREFP is ADC reference voltage
Sample frequence	SF_{adc}	1		400	Ksps	
Effective number of bits	$ENOB_{adc}$		12		bit	
Signal-to-noise and distortion ratio	$SINAD_{adc}$		74		dB	
Differential nonlinearity	DNL_{adc}	-3	± 2	3	LSB	
Integral nonlinearity	INL_{adc}	-4	± 2	4	LSB	

6 PCB Design

6.1 QFN60 Package

6.1.1 Package Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
b1	0.125REF		
c	0.20REF		
D	6.90	7.00	7.10
D2	5.25	5.40	5.55
Nd	5.55	5.60	5.65
e	0.40BSC		
E	6.90	7.00	7.10
E2	5.25	5.40	5.55
Ne	5.55	5.60	5.65
L	0.35	0.40	0.45
L1	0.10REF		
K	0.325	0.40	0.475
h	0.30	0.35	0.40
L/F载体尺寸 (MIL)	224*224		

Figure 6-1 QFN60 Package Dimension

6.1.2 Pin Layout

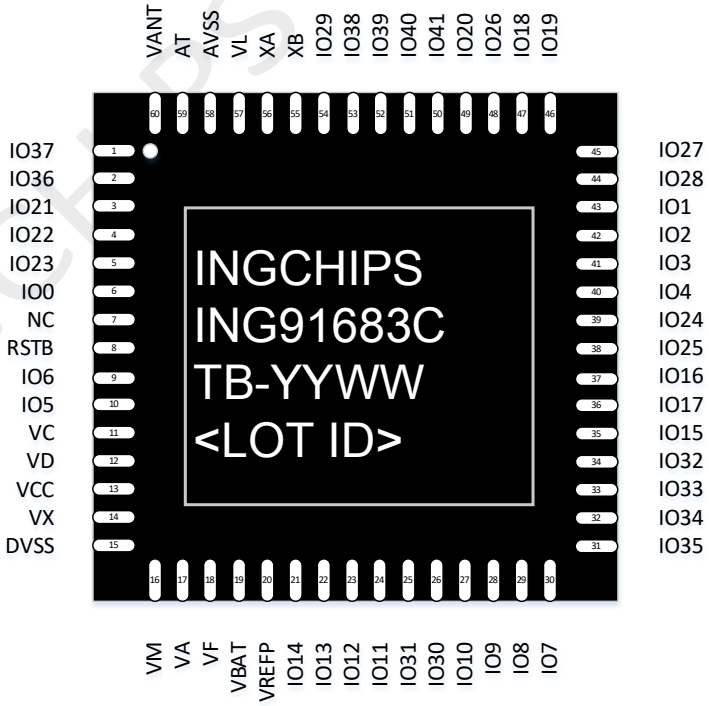


Figure 6-2 Pin Mapping of ING91683C

Table 6-1 ING91683C Pin Functions

No.	Pin Name	Type	Description
1	IO37	Digital I/O	GPIO
2	IO36	Digital I/O	GPIO
3	IO21	Digital I/O	GPIO
4	IO22	Digital I/O	GPIO
5	IO23	Digital I/O	GPIO
6	IO0	Digital I/O	GPIO
7	NC	-	Connect to ground
8	RSTB	Digital I/O	Chip reset, low active
9	IO6	Digital I/O, Analog	GPIO or 32.768KHz Crystal output
10	IO5	Digital I/O, Analog	GPIO or 32.768KHz Crystal input
11	VC	Power	Power decouple
12	VD	Power	Sense of switching regulator
13	VCC	Power	Supply for switching regulator
14	VX	Power	Switching regulator output
15	DVSS	Ground	Switching regulator ground
16	VM	Power	Power decouple
17	VA	Power	Power decouple
18	VF	Power	Power decouple
19	VBAT	Power	Battery voltage input
20	VREFP	Analog	ADC reference voltage
21	IO14	Digital I/O, Analog	GPIO or ADC AIN7
22	IO13	Digital I/O, Analog	GPIO or ADC AIN6
23	IO12	Digital I/O, Analog	GPIO or ADC AIN5
24	IO11	Digital I/O, Analog	GPIO or ADC AIN4
25	IO31	Digital I/O, Analog	GPIO or ADC AIN11
26	IO30	Digital I/O, Analog	GPIO or ADC AIN10
27	IO10	Digital I/O, Analog	GPIO or ADC AIN3
28	IO9	Digital I/O, Analog	GPIO or ADC AIN2
29	IO8	Digital I/O, Analog	GPIO or ADC AIN1
30	IO7	Digital I/O, Analog	GPIO or ADC AIN0
31	IO35	Digital I/O, Analog	GPIO or ADC AIN8
32	IO34	Digital I/O	GPIO
33	IO33	Digital I/O, Analog	GPIO or CMP VINN3
34	IO32	Digital I/O, Analog	GPIO or CMP VINN2
35	IO15	Digital I/O, Analog	GPIO or CMP VINN4
36	IO17	Digital I/O, Analog	GPIO or USB DM
37	IO16	Digital I/O, Analog	GPIO or USB DP
38	IO25	Digital I/O	GPIO
39	IO24	Digital I/O	GPIO
40	IO4	Digital I/O, Analog	GPIO or CMP VINP0
41	IO3	Digital I/O, Analog	GPIO or CMP VINN0
42	IO2	Digital I/O, Analog	GPIO or CMP VINP7
43	IO1	Digital I/O, Analog	GPIO or CMP VINP6
44	IO28	Digital I/O, Analog	High speed GPIO or CMP VINP5
45	IO27	Digital I/O, Analog	High speed GPIO or CMP VINP4
46	IO19	Digital I/O, Analog	High speed GPIO or CMP VINN1
47	IO18	Digital I/O, Analog	High speed GPIO or CMP VINP1
48	IO26	Digital I/O, Analog	High speed GPIO or CMP VINP3
49	IO20	Digital I/O, Analog	High speed GPIO or CMP VINP2
50	IO41	Digital I/O	GPIO
51	IO40	Digital I/O	GPIO
52	IO39	Digital I/O	GPIO
53	IO38	Digital I/O	GPIO
54	IO29	Digital I/O	GPIO

55	XB	Analog	Crystal 24MHz output
56	XA	Analog	Crystal 24MHz input
57	VL	Power	Power decouple
58	AVSS	Ground	Analog ground
59	AT	Analog	RF antenna pin
60	VANT	Power	RF bias voltage for antenna

6.2 Reference Design

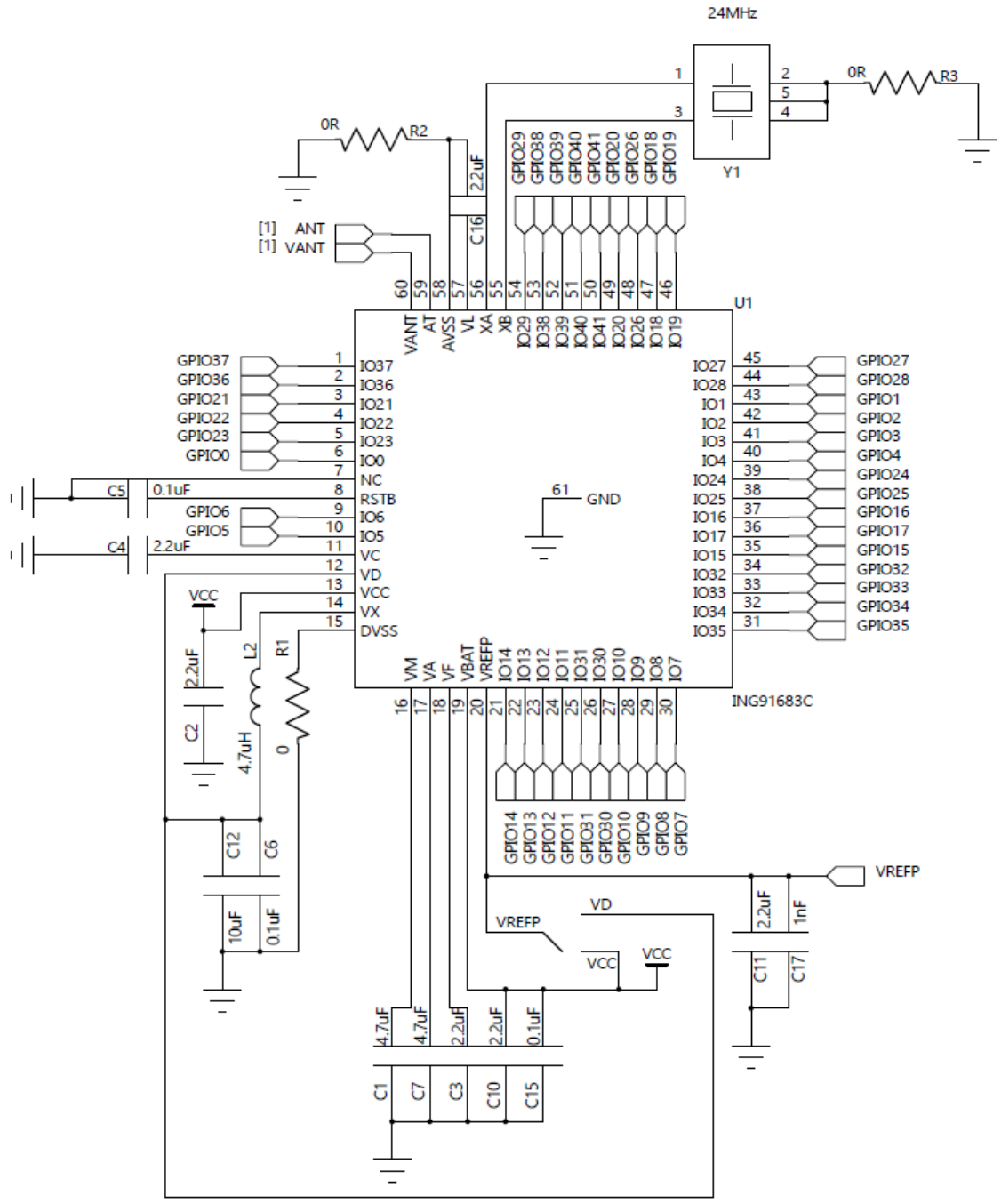


Figure 6-3 ING91683C Reference Design Schematic

Note: The Pin VREFP is the input reference voltage of ADC, the full scale range of ADC is from 0 to VREFP. According to the different accuracy requirements of ADC in the application, VREFP can be connected in many ways. Please contact Ingchips to get more application notes about the connection of VREFP.

6.3 RF matching network

The reference matching network as followed Figure 6-4, the component of matching network should be changed according user's board, as different board has different component's value for perfect performance. PCB board should keep enough keepout aera for antenna to abtain more antenna effciency.

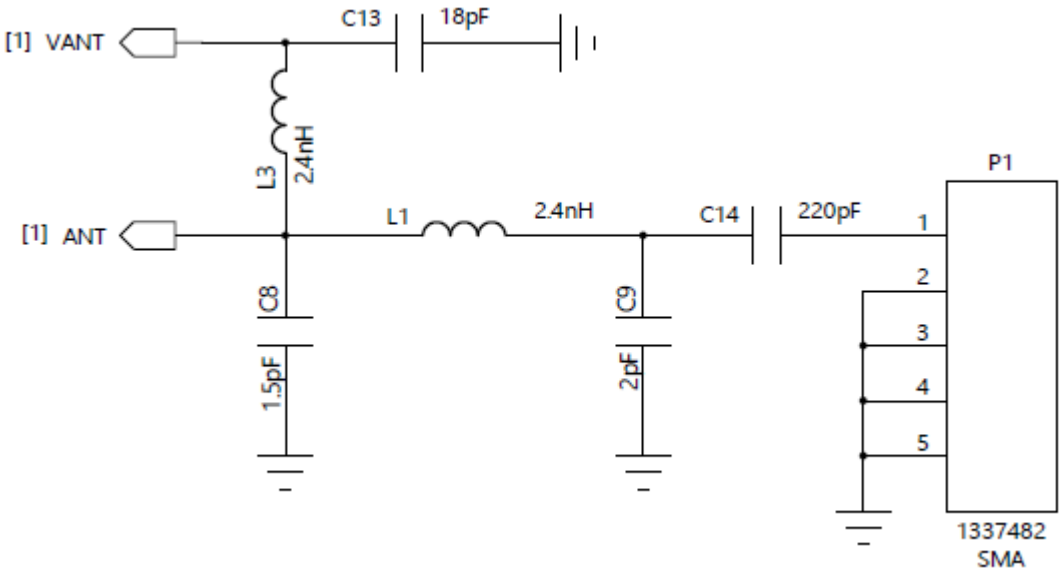


Figure 6-4 ING91683C RF Matching Network

6.4 PCB guideline

- Connect the decouple capacitors to power pins as close as possible, and use shortest and widest trace as possible, and following fan-out patter for capacitors is suggested.

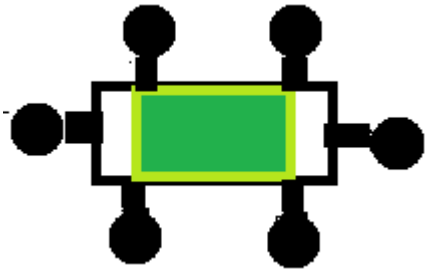


Figure 6-5 Fan-out Patter for Capacitors

- To switching regulator PCB layout, the circuit loop between input and output should be as small as possible, and meanwhile the input and output capacitor connected to ground using single point, SW away from sensitive analog areas.
- As to crystal, guard ring with unclosed around external signals XA/XB and external components is recommended, and return current across the crystal areas is forbidden. In multi-layer board application, it is recommended a ground plane layer under the top layer for better noise immunity.
- The matching network components, i.e., component relevant to the pin of VANT and ANT, should be soldered as close as possible to the chip.
- Impedance of 50ohms should be maintained in the route between the matching network and antenna. Notice that, in single layer application, coplanar model is used to calculate impedance.

7 Application Highlights

7.1 Direction Finding

The ING91683C supports for Direction Finding using BLE AoA or AoD method. By up to 75 antenna switching patterns, the chip can send and receive BLE Constant Tone Extensions in both advertising and connection modes. This makes it possible to do phase measurements on antenna arrays and ultimately to determine the direction of an incoming signal.

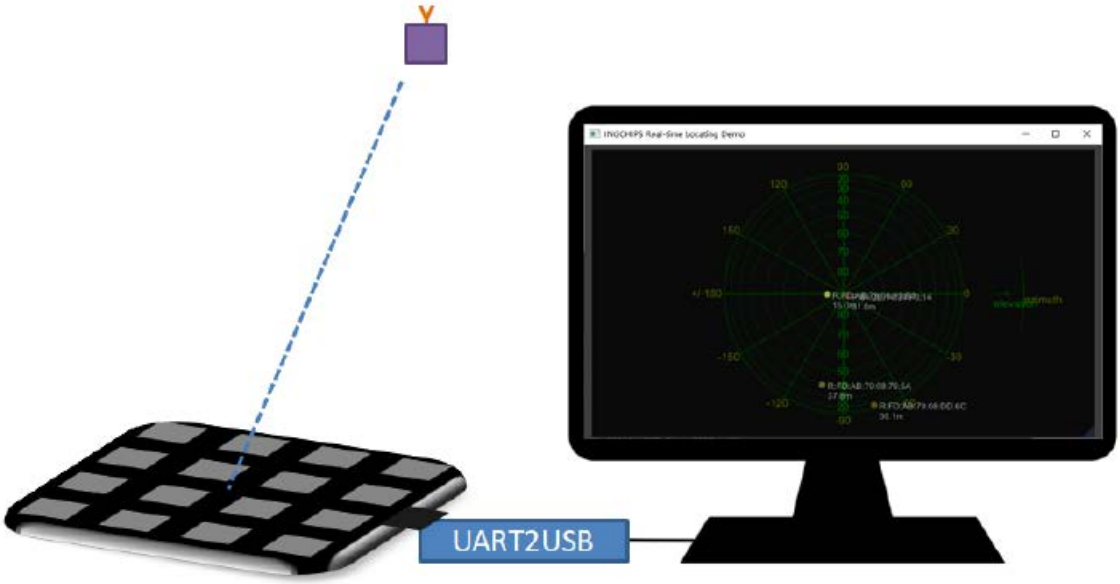


Figure 7-1 Direction Finding Test Platform

7.2 Long Range

The ING91683C supports BLE long range mode through LE Coded PHY, it can transmit data at a range for about four times comparing with the 1M PHY or 2M PHY.

This test example in SDK supports long range transmission:

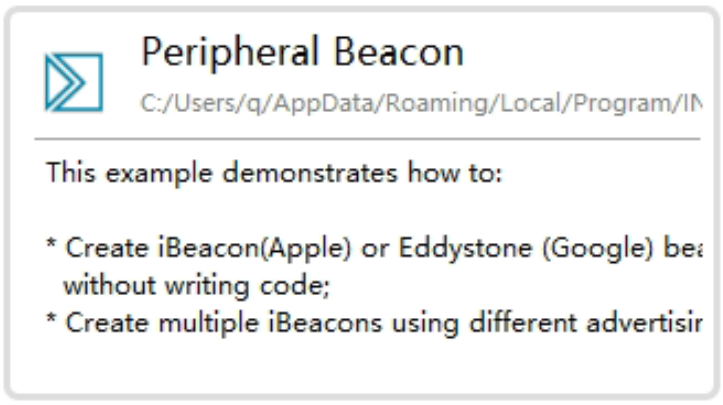


Figure 7-2 Test Example Supports Long Range in SDK

7.3 Multi-Connection

The ING91683C supports support multi-connection, master and slave in one device.

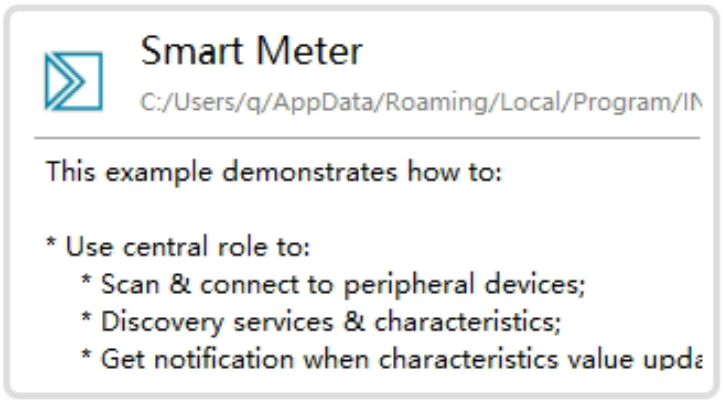


Figure 7-3 Test Example of Multi-connection in SDK

The example in SDK realizes a system with 4 thermo devices and 2 masters.

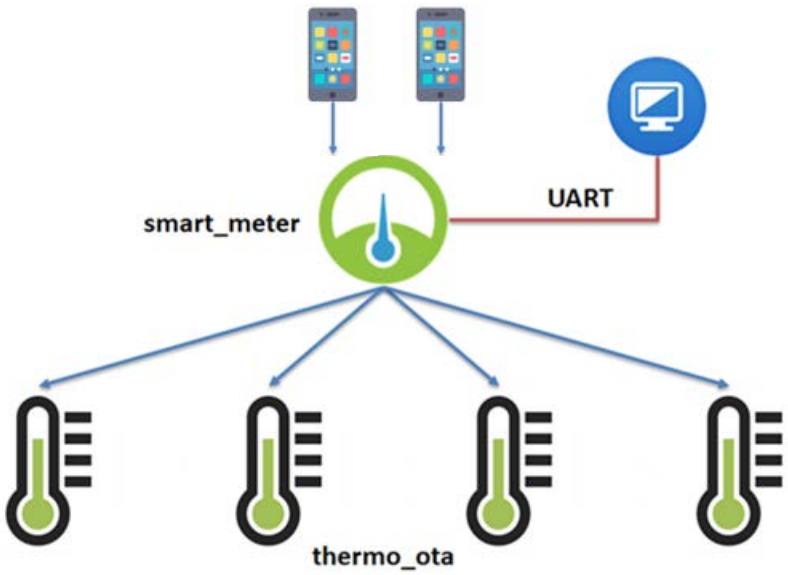


Figure 7-4 Diagram of Multi-connection

7.4 High Throughput

The ING91683C supports the throughput maximum to 1.2Mbps+.

Test examples are integrated in our SDK:

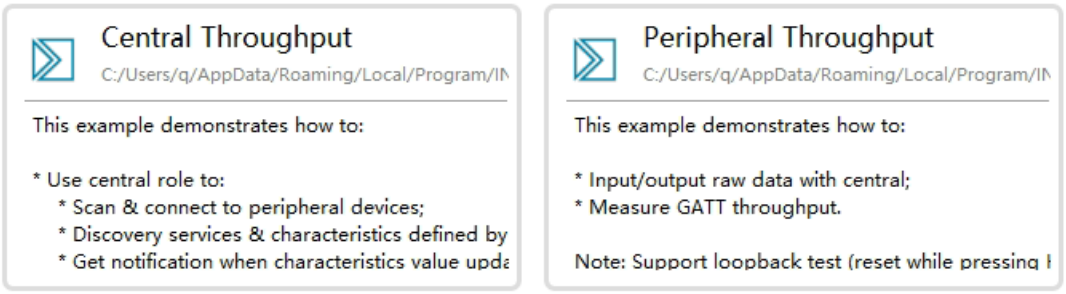


Figure 7-5 Test Examples of Throughout in SDK

The test result of throughout with mobilephone is as below:

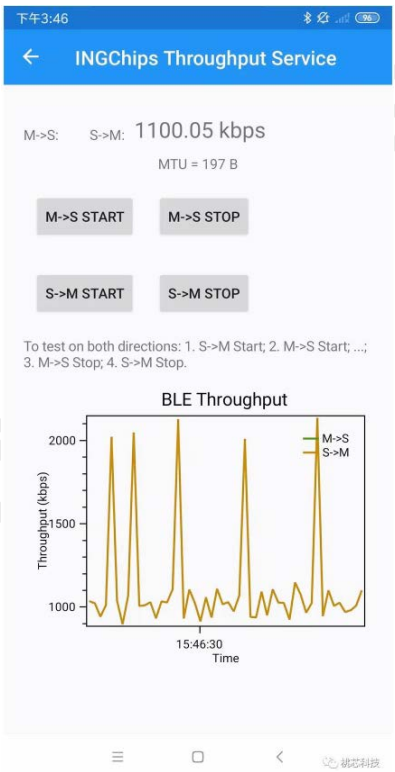


Figure 7-6 Throughput Test Result with Mobile Phone

Central_Throughput is a typical test case of BLE data transmission. The result is as below:

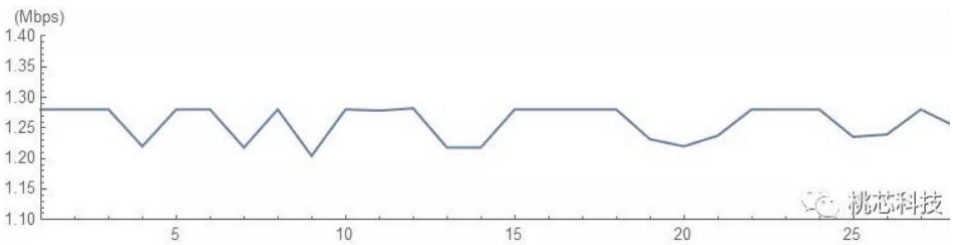


Figure 7-7 Test Result of Central_throughput

Update Records

Version	CR ID	Chapter	Page	Change Descriptions
1.0.0				Initial version
1.0.1	91683C.1	3.4.1	13	Change IO38/39/40/41 to support retention function only
		3.4.11	23	Add key Scanner matrix 16*20 and 20*16
1.0.2	91683C.2	3.4.3	16	Add LIN support in UART